REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are active in this application, Claims 1, 2, 4-10, 12, 14-16, and 20 having been amended by the present Amendment.

In the outstanding Office Action Claims 4, 5, 7-13, 15 and 16 were rejected under 35 USC §112, second paragraph, as being indefinite; and Claims 1-3, 6, 14 and 17-20 were rejected under 35 USC §103(a) as being unpatentable over Miyamoto et al (6,670,714).

In response to the rejection under 35 USC §112, second paragraph, Claim 1 has been amended to clarify that the recited via buried in the interlayer insulation layer is connected between an upper wiring layer and a first damaged region formed on the lower wiring layer, and that the dummy via buried in the interlayer insulation layer and not connected to the upper wiring layer is connected to a second damaged region formed on the lower wiring layer. Amended Claim 1 thus finds support, for example, in the embodiment of FIG. 2, wherein the damaged regions 15a and 15b are formed on the surface of the lower wiring layer 11, the via 14 is connected between the damaged region 15a and the upper wiring layer 12a, and the dummy vias 16 are connected between the damaged region 15b and the upper dummy wiring layer 19. Claims 4, 5, 7-13, 15 and 16 are also amended so as to be consistent with amended Claim 1 in accordance with U.S. claim drafting practice, thereby to recite the above-mentioned feature more clearly. Thus, in the amended claims, it is clear that the dummy via is not located remotely from the lower wiring layer but located nearly to the lower wiring layer so that the dummy via is connected to a damaged region formed in the lower wiring layer, consistent with the supporting disclosure. Accordingly, no new matter has been added, and it is respectfully submitted that the outstanding rejection under 35 USC §112, second paragraph, has been overcome.

Turning now to the outstanding rejection of Claims 1-3, 6, 14, 17-20 as being obvious over Miyamoto et al , in FIG. 5D Miyamoto et al show a first metal interconnection 19, a via contact 21 and a second metal interconnection 22 respectively corresponding to the lower wiring layer, via and an upper wiring layer recited in Claim 1, for example. The outstanding Office Action states a position that vias buried in the interlayer insulation layer in the left side of the multi-wiring structure shown in FIG. 5D of Miyamoto et al are dummy vias. However, Applicants respectfully dispute this finding since Miyamoto et al are silent as to whether or not these vias are dummy vias. Applicants think not, since these vias are not connected to a lower wiring layer, unlike the present invention recited in Claim 1, for example.

On the other hand, in FIG. 7 and the corresponding description at column 5, line 66 to column 6, line 6, Miyamoto et al disclose that a plurality of via contacts 32a (two in FIG. 7) are arranged to connect the lower interconnection 31 to the upper interconnection 32. All of these via contacts 32a are connected between the lower and upper interconnections. Therefore, none of these via contacts 32a is a dummy via and no dummy via is connected to the lower interconnection 31, once again, unlike the claimed invention.

In fact, Miyamoto et al at column 7, lines 50-55 teach that when the width W of the lower interconnection 31 exceeds a given value X (W>X), two or more via contacts 32a may be arranged in order to prevent a contact failure from being occurred and to improve the dependence of the failure rate on the width of the interconnection more greatly. However, this contact arrangement using two or more via contacts will cause contact defects (disconnection or open defects) of at least one or more via contacts, as described by Applicants in the description of the related art at pages 1-7, and particularly at page 7, lines 3-6, of Applicants' specification.

On the contrary, according to the present invention recited in Claim 1, for example, the probability of occurrence of the open defects on the via or vias (used as signaling vias)

can be lowered by additionally providing the dummy via or vias. Provided that two signaling vias are provided on a wide lower wiring layer, and a sufficient number of dummy vias are designed, no open defect of the two signaling vias will occur according to Applicants' invention. In contrast, in the case of the circuit device taught by Miyamoto et al, there is a possibility of occurrence of an open defect with respect to at least one of two signaling vias 32a, since no dummy via is provided therein.

To highlight the above discussed distinction, independent Claims 1, 14, 20 have been amended to accentuate that a via is connected to a lower wiring layer and a dummy via is also connected to this structural feature is neither taught nor suggested by Miyamoto et al., it is respectfully submitted that the outstanding rejection on the merits has been overcome.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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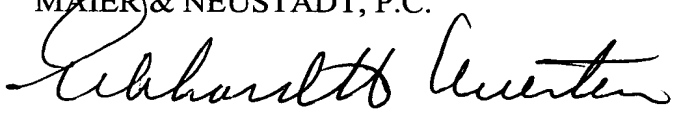

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